

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In application of: RAMINDA U. MADURAWE  
Application No.:  
Title: Integrated Circuits with RAM and ROM Fabrication Options  
Filed: 12/31/2003

INFORMATION DISCLOSURE STATEMENT SUBMISSION

Sirs:

Attached is IDS form 1449 along with copies of the references for the Application submitted herewith entitled "Integrated Circuits with RAM and ROM Fabrication Options".

Regards,

Raminda Madurawe  
Raminda U. Madurawe

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Commissioner for Patents  
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on December 31, 2003

By:

Raminda Madurawe  
Raminda U. Madurawe

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PTO/SB/08A (08-00)

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<p>Substitute for form 1449A/PTO</p> <h2 style="text-align: center;">INFORMATION DISCLOSURE STATEMENT BY APPLICANT</h2> <p><i>(use as many sheets as necessary)</i></p>				<b>Complete if Known</b>	
				<b>Application Number</b>	
				<b>Filing Date</b>	12/31/2003
				<b>First Named Inventor</b>	Madurawwe, Raminda U.
				<b>Group Art Unit</b>	
				<b>Examiner Name</b>	
				<b>Attorney Docket Number</b>	
Sheet	1	of	2		

## **U.S. PATENT DOCUMENTS**

## **FOREIGN PATENT DOCUMENTS**

<b>Examiner Signature</b>		<b>Date Considered</b>	
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<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	
Sheet	2	of	2	Filing Date	12/31/2003
				First Named Inventor	Madurawe, Raminda U.
				Group Art Unit	
				Examiner Name	
				Attorney Docket Number	

<b>OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS</b>			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		SEALS & WHAPSHOT, "Programmable Logic – PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA	<input type="checkbox"/>
		ASHOK K. SHARMA, "Programmable Logic Handbook – PLDs, CPLDs, & FPGAs", 1998, pp 99-171, McGraw-Hill, USA	<input type="checkbox"/>
		S. M. SZE, "VLSI Technology", 1983, pp 600-609, McGraw-Hill, New York, USA	<input type="checkbox"/>
			<input type="checkbox"/>

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